



OVERVIEW

Myrmidon is a PCIe card designed to handle the rigorous requirements of modern video codecs. At the heart of the card is Xilinx Kintex Ultrascale FPGA. Three banks of DDR4 memory provide memory storage and bandwidth for processing compressed and baseband UHDp60 video. Two expansion connectors can be populated with daughter cards that enable audio processing and provide interfaces such as ASI, 12G SDI or 10-G Ethernet. The card is designed such that when decoding compressed content the FPGA can identify the video format employed and reconfigure itself to match the input format.

FEATURES

FPGA	Xilinx Kintex Ultrascale-XCKU040-1TFFVA1156
Memory	Bank 1:80-bit wide 2.5 Gbyte DDR4 at 1GHz [5x16 components each of 4Gb density] Bank 2:80-bit wide 2.5 Gbyte DDR4 at 1GHz [5x16 components each of 4Gb density] Bank 3:48-bit wide 2.5 Gbyte DDR4 at 1GHz [3x16 components each of 4Gb density]
On Board Clock	156.25 MHz and 100 MHz oscillators Video clock generator with 27 MHz, 148.5 and 148.35 MHz clocks 3-PLL 3 output programmable clock generator
Configuration	1 GByte x16BPI flash Configuration control from FPGA, on board switches or expansion connectors
Interfaces	PCIe Gen 3 4-lane Expansion Connector 1 [Samtec SEAF 20x10] ▪ 32 I/O ▪ 8 clocks ▪ 10 Gigabit trasceivers Expansion Connector 1 [Samtec SEAF 20x10] ▪ 32 I/O ▪ 8 clocks ▪ 10 Gigabit trasceivers JTAG
Power	12 V 5A input Provision for up to 40 A for FPGA
Dimensions	250mm x 107mm x 25mm

VIDEO CORES SUPPORTED

Decoding

- MPEG -2 422 8 -bit – 8 channels of HDp60
- AVC 422 10 -bit – 4 channels of HDp60 or 1 channel of 4Kp60
- HEVC 422 12 -bit – 4 channels of HDp60 or 1 channel of 4Kp60
- HEVC 444 12 -bit – 2 channels of HDp60 or 1 channel of 4Kp30

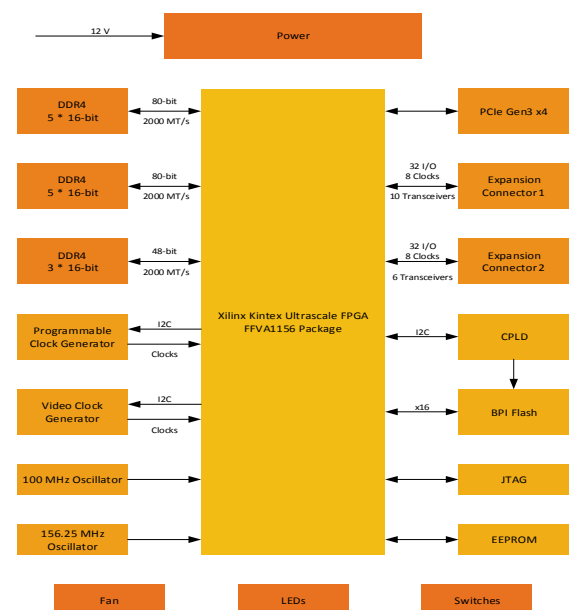
Encoding

- AVC Intra Frame 422 10 - bit - 4 channels of HDp60 or 1 channel of 4Kp60

HARDWARE VIEW



BLOCK DIAGRAM



RELATED OFFERINGS

Hardware

- Schematics, PCB Layout, BOM

Software (source code or netlist)

- MPEG-2 Decoder FPGA IP core
- AVC Decoder FPGA IP core
- AVC Intra Frame Encoder FPGA IP core
- HEVC Decoder FPGA IP Core



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